



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Akira SAKAI et al.

Group Art Unit: 2826

Application No.: 10/807,235

Examiner: E. PERT

Filed: March 24, 2004

Docket No.: 119232

For: METHOD FOR FABRICATING A METALLIC OXIDE OF HIGH DIELECTRIC CONSTANT, METALLIC OXIDE OF HIGH DIELECTRIC CONSTANT, GATE INSULATING FILM AND SEMICONDUCTOR ELEMENT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection, Notice of Allowance, or other action that closes prosecution (e.g., Quayle Action), but before payment of the Issue Fee. Attached is our Check No. 172363 in the amount of \$180.00 in payment of the fee under 37 CFR §1.17(p). Please credit or debit Deposit Account No. 15-0461 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.
- a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.  
37 CFR §1.97(e)(1).
- 2. The references were cited in a counterpart foreign application. An English language version of the foreign search report is attached for the Examiner's information.
- 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

4. In accordance with the September 21, 2004 Commissioner's Notice, copies of pending U.S. patent applications filed on or after June 30, 2003, or entering the U.S. National Stage after June 30, 2003, are not attached.

Respectfully submitted,

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Date: October 31, 2005

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<b>DEPOSIT ACCOUNT USE AUTHORIZATION</b> Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461
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Sheet 1 of 1

Form PTO-144 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 119232	APPLICATION NO. 10/807,235		
INFORMATION DISCLOSURE STATEMENT  (Use several sheets if necessary)						
		APPLICANT(S) Akira SAKAI et al.				
		FILING DATE March 24, 2004	GROUP 2826			
U.S. PATENT DOCUMENTS						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1.	6,509,283	01-21-2003	Thomas		
	2.	2003/0020068 A1	01-30-2003	Finder		
	3.	2002/0197793 A1	12-26-2002	Dornfest et al.		
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)						
	4.	European Search Report dated September 19, 2005				
	5.	Osten, et al., <u>Epitaxial Praseodymium Oxide: A new high-K dielectric</u> , pp. 100-106, JWGI (2001)				
	6.	<u>Liu, et al., Epitaxial growth of Pr<sub>2</sub>O<sub>3</sub> on Si(111) and the observation of a hexagonal to cubic phase transition during postgrowth N<sub>2</sub> annealing</u> , 79(5):671-673, Applied Physics Letters (July 30, 2001)				
	7.	<u>Ferrari, et al., Chlorine mobility during annealing in N<sub>2</sub> in ZrO<sub>2</sub> and HfO<sub>2</sub> films grown by atomic layer deposition</u> , 92(12):7675-7677, J. of Applied Physics (December 15, 2002)				
	8.	<u>Murawala, et al., Plasma Enhanced Liquid Source-CVD and Rapid Thermal Annealing of Tantalum Penta Oxide Dielectric Material</u> , Materials, Tsukuba, pp. 527-529 (1992)				
	9.	<u>Mereu, et al., Fowler-Nordheim Tunneling in Epitaxial Yttrium Oxide on Silicon for High-K Gate Applications</u> , Proceedings of the IEEE International Semiconductor Conference, 2:309-312 (October 8, 2002)				
EXAMINER					DATE CONSIDERED	
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						